



Docket No.: 42390P7045D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

SURESH RAMALINGAM, ET AL.

Application No.: 09/874,666

Filed: June 5, 2001

For: **A Controlled Collapse Chip Connection
(C4) Integrated Circuit Package Which
Has Two Dissimilar Underfill Materials**

Art Group: 2827

Examiner: David E. Graybill

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

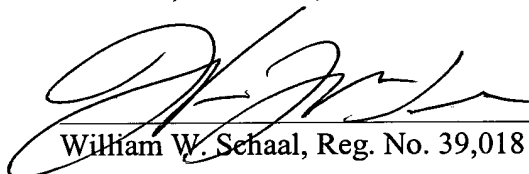
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

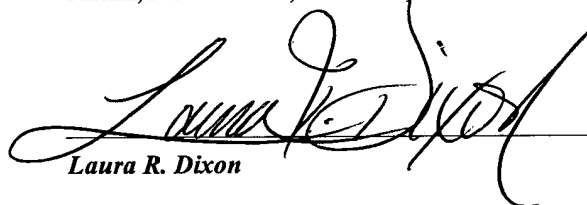
Date: August 22, 2003



William W. Schaal, Reg. No. 39,018

12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025
(714) 557-3800

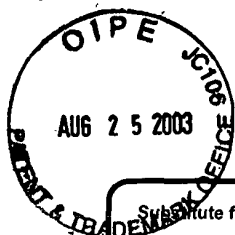
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Laura R. Dixon

08-22-03

Date



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|--|---|----|---|--------------------------|-------------------|
| Substitute for form 1449A/PTO | | | | Complete if Known | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | Application Number | 09/874,666 |
| | | | | Filing Date | June 5, 2001 |
| | | | | First Named Inventor | Suresh Ramalingam |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | David E. Graybill |
| Sheet | 1 | of | 1 | Attorney Docket Number | 42390P7045D |

| OTHER ART - NON PATENT LITERATURE DOCUMENTS | | | |
|---|--------------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | A | SUMITA K. ET AL. "High Reliability Underfill for Flip-Chip Application" 1997, Materials Research Society Symposium Proceedings XP-000912270 abstract. | |
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.
Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450